ABSTRACT OF THE DISCLOSURE

A memory cell is constituted by a TMR element and a MOS transistor. The source diffusion layer of the MOS transistor is connected to a source line and the drain diffusion layer of the transistor is connected to a TMR element via a local interconnection wire. The TMR element is held between the local interconnection wire and a bit line. The TMR element is constituted by stacked TMR layers. Each TMR layer is able to have two states, that is, a state in which spin directions are parallel and anti-parallel. Therefore, the TMR element stores four-value data. A current-driving line is set immediately below the TMR element.